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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,494	07/01/2003	Jun-Young Lee	50391/DBP/Y35	4433

23363 7590 07/26/2006

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EXAMINER	
MOON, SEOKYUN	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,494	LEE, JUN-YOUNG	
	Examiner	Art Unit	
	Seokyun Moon	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7 and 9-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4-7,9,11,13-15,and17* is/are rejected.

7)☒ Claim(s) *2,10,12,16 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statements (IDS) filed on July 01, 2003 and February 02, 2005 have been acknowledged and considered by examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1, 5-7, 9, 11,** and **13-15** are rejected under 35 U.S.C. 102(b) as being anticipated by Kishi et al. (EP 1,065,650 A2, herein after referred to as "Kishi").

As to **claim 1**, Kishi [fig. 62] teaches an apparatus for driving a plasma display panel, which has a panel capacitor ("*Co*"), the apparatus comprising:

a first switch ("*SW5*") and a second switch ("*SW3*") being coupled in series between a first power source ("*ground*") for supplying a first voltage ("*0*") and a first terminal of the panel capacitor;

a third switch ("*SW4*") and a fourth switch ("*SW1*") being coupled in series between the first terminal of the panel capacitor and a second power source ("*1/2Vs*") for supplying a second voltage;

a first capacitor coupled between a common contact between the first switch and the second switch and a common contact between the third switch and the fourth switch; and

a fifth switch ("*SW2*") coupled between the first capacitor ("*C1*") and a third power source ("*ground*") supplying a third voltage ("*0*").

wherein the third voltage is substantially a ground voltage.

As to **claim 5**, Kishi [fig. 62] teaches the first switch, the second switch, the third switch, and the fourth switch, each has a body diode.

As to **claim 6**, Kishi teaches the apparatus, further comprising:

a sixth switch ("*SW5'*") and a seventh switch ("*SW3'*") being coupled in series between the first power source ("*ground*") and a second terminal ("*Y*") of the panel capacitor;

an eighth switch ("*SW4'*") and a ninth switch ("*SW1'*") being coupled in series between the second terminal of the panel capacitor and the second power source ("*1/2 Vs*");

a second capacitor ("*C4*") coupled between a common contact between the sixth switch and the seventh switch and a common contact between the eighth switch and the ninth switch; and

a tenth switch ("*SW2'''*") coupled between the second capacitor and the third power source ("*ground*").

As to **claim 7**, Kishi [fig. 62] teaches an apparatus for driving a plasma display panel, which has a panel capacitor ("*Co*"), the apparatus comprising:

a first switch ("*SW5*") and a second switch ("*SW3*") being coupled in series between a first power source ("*ground*") for supplying a first voltage ("*0*") and a first terminal of the panel capacitor;

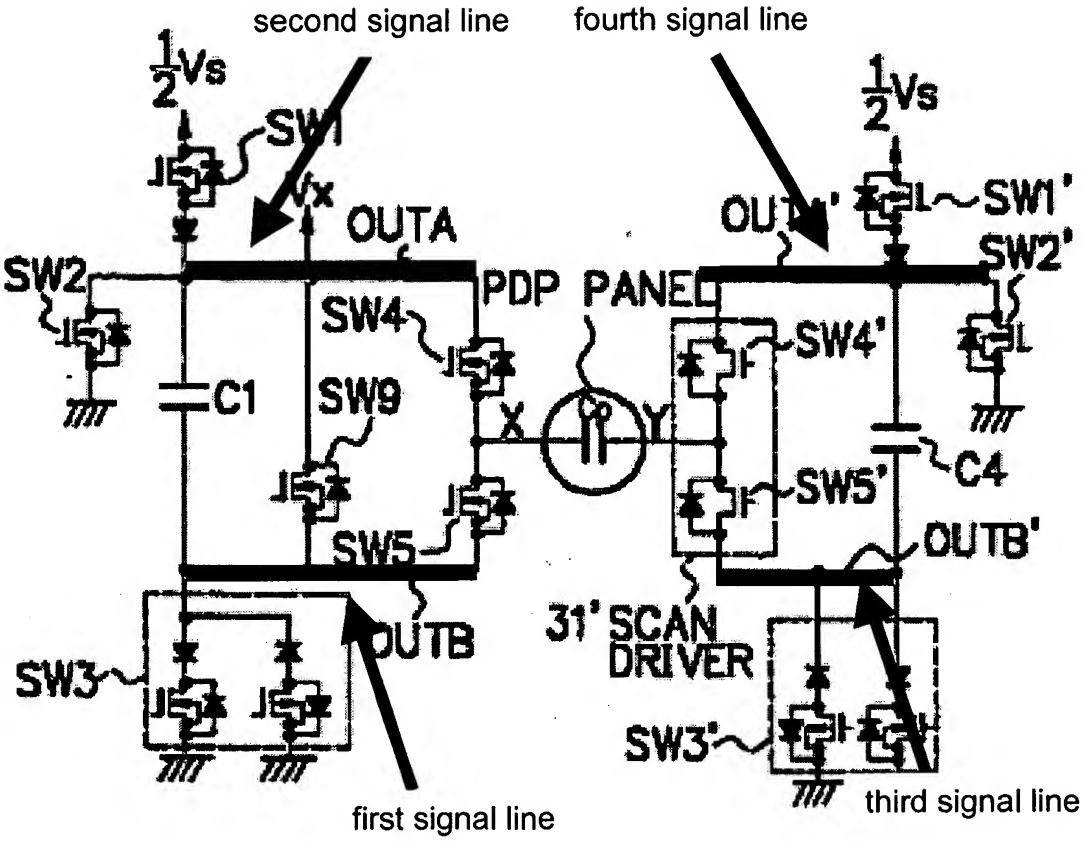
a third switch ("*SW4*") and a fourth switch ("*SW1*") being coupled in series between the first terminal of the panel capacitor and a second power source ("*1/2Vs*") for supplying a second voltage;

a first signal line coupled to a common contact between the first switch and the second switch [drawing 1 provided below, which is equivalent to Kishi's fig. 62]; and

a second signal line coupled to a common contact between the third switch and the fourth switch,

wherein a voltage between the first signal line and the second signal line is a third voltage ("*1/2Vs*"), the first voltage and the second voltage are alternatively applied to the first terminal of the panel capacitor, and

wherein a ground voltage is applied to the first signal line while the second voltage ("*1/2Vs*") is applied to the first terminal of the panel capacitor.



Drawing 1

As to **claim 9**, Kishi teaches a capacitor ("*C1*") between the first signal line and the second signal line and charged to the third voltage ("*1/2 Vs voltage*").

As to **claim 11**, Kishi does not teach a power recovery section charging a terminal voltage of a panel capacitor using a resonance generated between an inductor and the panel capacitor.

However, Ohba teaches the apparatus ("*plasma display panel driver circuit*") comprising a power recovery section (the part comprising *FET switches 30, 32*, *diodes 31, 33*, and *capacitor 29* of the *plasma display panel driver circuit* shown in *fig. 3*)

including at least one inductor ("*34*") coupled to the first terminal of the panel capacitor ("*40*"), the power recovery section changing a terminal voltage of the panel capacitor using a resonance generated between the inductor and the panel capacitor [*fig. 3*].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include Ohba's power recovery section in Kishi to reduce the power consumption in display driving circuit [Ohba: *col. 2 lines 47-49*].

As to **claim 13**, all of the claim limitations have already been discussed with respect to the rejection of claim 5.

As to **claim 14**, Kishi [fig. 62] teaches the apparatus, further comprising:

a fifth switch ("*SW5*") and a sixth switch ("*SW3*") being coupled in series between the first power source ("*ground*") and a second terminal ("*Y*") of the panel capacitor;

a seventh switch ("*SW4*") and an eighth switch ("*SW1*") being coupled in series between the second terminal of the panel capacitor and the second power source ("*1/2Vs*");

a third signal line coupled to a common contact between the fifth switch and the sixth switch [drawing 1 provided on page 5 of this office action]; and

a fourth signal line coupled to a common contact between the seventh switch and the eighth switch,

wherein a voltage between the third signal line and the fourth signal line is the third voltage ("*1/2 Vs*"), and the second voltage is applied to the second terminal of the panel capacitor while the first voltage is applied to the first terminal of the panel

capacitor, and the first voltage is applied to the second terminal of the panel capacitor while the second voltage is applied to the first terminal of the panel capacitor.

As to **claim 15**, Kishi [fig. 62] [drawing 1 provided on page 5 of this office action] teaches a method for driving a plasma display panel, by alternatively applying a first voltage ("*1/2Vs*") and a second voltage ("*ground*") respectively through a first signal line and a second signal line both coupled to a first terminal ("*X*") of a panel capacitor ("*Co*"), a first common contact being formed between a first switch and a second switch located between a third switch and a fourth switch located on the second signal line, the method comprising:

applying the first voltage ("*1/2Vs*") to the first terminal of the panel capacitor by turning on the first switch ("*SW4*") and the second switch ("*SW1*"), while a third voltage is applied between the first common contact and the second common contact;

applying the second voltage ("*ground*") to the first terminal of the panel capacitor by turning on the third switch ("*SW5*") and the fourth switch ("*SW3*") while the third voltage is applied between the first common contact and the second common contact, and

applying a ground voltage to the first common contact while the second voltage is being applied to the first terminal of the panel capacitor.

5. **Claims 4** and **17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishi in view of Ohba et al. (US pat. no. 5,670,974, herein after referred to as "Ohba").

As to **claim 4**, Kishi does not expressly teach the apparatus comprising at least one inductor, a sixth switch, and a seventh switch, wherein the sixth switch and the seventh switch being coupled in parallel between the inductor and a third power source.

However, Ohba [fig. 3] teaches the apparatus ("*plasma display panel driver circuit*") comprising:

at least one inductor ("*34*") coupled to the first terminal of the panel capacitor ("*40*"); and

a sixth switch ("*30*" + "*31*") and a seventh switch ("*32*" and "*33*") being coupled in parallel between the inductor and the third power source ("*(1/2)Vs*" + "*28*").

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include the part comprising *FET switches 30, 32*, *diodes 31, 33*, and *capacitor 29* of the *plasma display panel driver circuit* of Ohba, in Kishi to reduce the power consumption in display driving circuit [Ohba: *col. 2 lines 47-49*].

As to **claim 17**, Kishi modified by Ohba [Kishi: fig. 62] [Ohba: fig. 3] teaches the method, wherein

applying the first voltage (Kishi: "*1/2Vs*") to the first terminal (Kishi: "*X*") of the panel capacitor further includes raising a voltage of the first terminal of the panel capacitor to the first voltage using a first resonance generated between an inductor (Ohba: "*81*") coupled to the first terminal of the panel capacitor before the first voltage is applied to the first terminal of the panel capacitor ("*Ohba 82*"),

wherein applying the second voltage ("*ground*") to the first terminal of the panel capacitor further includes dropping the voltage of the first terminal of the panel capacitor

to the second voltage using a second resonance generated between the inductor and the panel capacitor before the second voltage is applied to the panel capacitor.

Allowable Subject Matter

6. **Claims 2, 10, 12, 16,** and **18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims **1, 7,** and **15** have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

July 22, 2006
S.M.

AMR A. AWAD
PRIMARY EXAMINER